Abstract

The present invention provides an algorithm and hardware structure for numerical operations on signals that is reconfigurable to operate in a downsampling or non-downsampling mode. According to one embodiment, a plurality of adders and multipliers are reconfigurable via a switching fabric to operate as a plurality of MAAC kernels (described in detail below), when operating in a non-downsampling mode and a plurality of MAAC kernels and AMAAC kernels (described in detail below), when operating in a downsampling mode.